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Suitability of Voltage Sensors for the Measurement of Switching Voltage Waveforms in Power Semiconductors

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ABSTRACT This paper investigates the effect of voltage sensors on the measurement of transient voltages for power semiconductors in a Double Pulse Test (DPT) environment. We adapt previously published models that were developed for current sensors and apply them to voltage sensors to evaluate their suitability for DPT applications. Similarities and differences between transient current and voltage sensors are investigated and the resulting methodology is applied to commercially available and experimental voltage sensors. Finally, a selection aid for given measurement tasks is derived that focuses on the measurement of fast-switching power semiconductors.

INDEX TERMS Double pulse test, error analysis, measurement errors, power semiconductors, sensor phenomena and characterization, voltage measurement, wide band gap.

I. INTRODUCTION

Measuring and minimising wide band gap (WBG) power semiconductor switching losses has been a research topic for several years. Low switching losses are desirable to implement higher switching frequencies in power electronic converters so that their size and weight can be minimised. However, as switching losses decrease, the precision of the measurement system, its deskew alignment and its unintended influence on the test circuit become more and more relevant. These effects have to be considered especially for Gallium Nitride (GaN) devices, yet Silicon Carbide (SiC) power semiconductors and Silicon (Si) MOSFETs are affected as well. A widely accepted method to measure switching losses in power semiconductors is the Double Pulse Test (DPT, Fig. 1) which requires the simultaneous measurement of the device switching current and its switching voltage.

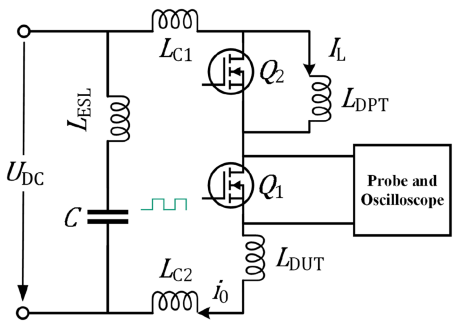


FIGURE 1. Generic Double Pulse Test Setup with identical MOSFETs Q_1 (DUT) and Q_1. C: DC-link capacitance. L_{ESL}: Equivalent series inductance of the DC-link capacitance. L_{C1} and L_{C2}: Parasitic connection inductances. L_{DPT}: DPT load/storage inductor. L_{DUT}: Parasitic device inductance.

As described in [1], two main problems regarding the measurement of fast transients can be identified:

- Capacitive coupling between the measurement equipment and the device under test (DUT), influenced by steep $^{du}/_{dt}$ slopes exceeding 100 $\frac{\mathrm{V}}{\mathrm{ns}}$ without much effort in contemporary WBG power semiconductors
- Inductive influences through current sensors inserted into the DUT switching cell, influenced by steep $^{di}/_{dt}$ slopes in the range of several tens or even hundreds $\frac{\mathrm{A}}{\mathrm{ns}}$.

General guidelines to select, calibrate and connect voltage probes to a DPT circuit are presented in [2]. They describe the properties of the probe, such as bandwidth, rise time, parasitic capacitance and connector inductance, and provide suggestions to match a probe to the intended DUT circuit. The parasitic effects of voltage probes on switching waveforms were analysed more precisely in [3]. This analysis focused on high-voltage probes for several hundred Volts up to a few tens of kV, on the resonance between the parasitic commutation inductance of the DPT circuit and the device / sensor capacitances, and on the derivation of design guidelines for passive voltage probes. A design for a passive sensor was presented and compared to commercially available voltage probes with larger input capacitances. A clear effect of the probe on the switching waveform was reported, again pointing out the necessity to account for the measurement setup in WBG DPTs.

However, a general comparison or method to rate voltage sensors regarding their viability for fast transient measurements has not been presented. Such a method was developed for *current sensors* in [1], allowing a general mathematical error description that takes both DUT circuit parameters and the properties of the used sensor into account.

This article now focuses on the development of an analogous methodology for *voltage sensors* to identify their possible (and probable) influences on a DPT setup, completing the investigation of the two most dominant and important changes between a DUT in an application circuit and in a DPT circuit. In addition to the description of the identified influences, a selection aid that enables a quick worst-case error estimate for exemplary voltage probes is developed as well.

This article is structured as follows: Section II reviews the applied method in [1] and adapts it to voltage sensors. Section III provides a brief overview of available sensor types while Section IV uses the developed mathematical descriptions to analyse available voltage sensors to evaluate their suitability for WBG DPTs. Section V summarises the results and provides an outlook onto further research topics.

II. SUMMARY AND ADAPTATION OF PREVIOUS INVESTIGATIONS

The influences of current sensors on WBG DPTs were investigated in [1]. For an ideal measurement, any influence on the DUT would have to be avoided, however small it may be. With real probes hoewever, such an ideal measurement is not possible since every probe needs some kind of coupling to the DUT, be it through direct insertion, inductive or capacitive coupling. This investigation therefore inspected the parasitic effects of current sensors more cloesly, revealing a twofold influence on fast transient currents:

1) The parasitic inductance added through the insertion of the sensor lowers the $^{di}/_{dt}$ current slope of the DUT immediately after turn-on and increases the current rise time of the semiconductor.
2) The transformation of the current flowing through the DUT to an output voltage at the contacts of the sensor imposes a low-pass filter effect on the current waveform, reducing the high-frequency components of the measurement signal.

It was shown that these influences form a chain of errors, stacking their individual contributions so that the total error of the current measurement can be quite substantial, depending on the combination of DUT and sensor.

A similar analysis can be performed for voltage probes. In an ideal setup, also voltage measurements should have no influence on the DUT. Yet again, real voltage probes cannot fulfil this idealised requirement. Different to current sensors hoewever, their introduction into a DPT circuit does not change the current path, but increases the (parasitic) capacitance in parallel to the DUT channel.

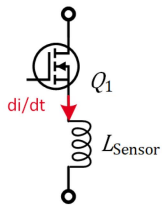
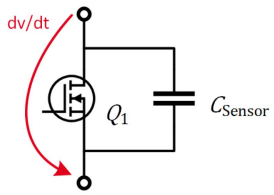
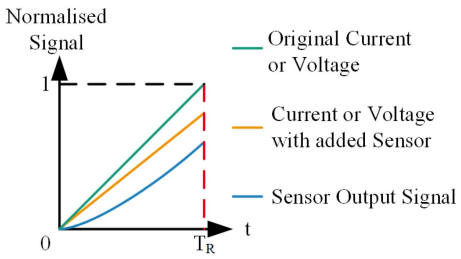
An overview of the commonalities and differences between the application of current and voltage probes in a DPT is provided in Table 1. In the following subsections, the influences of voltage probes on the measurement of transient voltages are analysed in detail.

A. INFLUENCE OF VOLTAGE PROBES ON TRANSIENT VOLTAGE MEASUREMENTS

When a power semiconductor is switched off, the voltage across its channel contacts will rise from the on-state voltage, which is close to 0 V, up to the applied DC voltage and, for a transient period, also exceed it due to the inductive turn-off overvoltage. For practical applications, the rate of this voltage rise is dominated by "internal" factors of the DUT, such as channel transition time and parasitic capacitance, but can also be influenced through "external" factors, such as the layout of the commutation loop, the behaviour of the commutation partner and the gate network. Since this work aims at a worst-case estimate of the influence of voltage sensors on the measurement of fast voltage transients, ideal DUT channels ($R_{\mathrm{DS,on}} = 0$) with infinitely fast transition times as well as sufficiently well designed commutation loops and commutation partners are assumed. With these assumptions, the voltage rise across the DUT is solely dependent on the capacitances of the DUT.

This assumption is certainly excessively idealised for slow-switching, high-voltage and/or high-current power semiconductors, since such devices usually exhibit far-from-ideal switching behaviour. However, measuring the switching losses of such devices is relatively easy in comparison to fast-switching, lower-voltage and/or lower-current devices due to the much larger packages, longer switching time and component parasitics. In contrast, fast-switching devices, e.g. GaN

TABLE 1. Comparison Between the Influences of Current Sensors on the Measurement of Transient Currents and the Influences of Voltage Sensors on the Measurement of Transient Voltages

Physical influence		Measurement influence
Current Sensors	**Voltage Sensors**	**All Sensors**
Added inductance in the commutation loop	Added capacitance in parallel to the DUT	Distortion of the sensor output signal due to low-pass characteristic of the sensor
		

High Electron Mobility Transistors (HEMTs), are approaching or even going below single-digit nanosecond transition times [5], depending on their voltage class and operating point. This assumption is therefore usable to create a reasonable worst-case estimate of the influence of the probe on the DUT.

In a regular circuit, i.e. a circuit *without* a connected voltage probe, a turn-off switching event will charge the output capacitance C_{OSS} of the DUT according to (1), T_R being the voltage rise time of the switching event.[1] In general, the capacitive current i_C will be nonlinear since the output capacitances of power semiconductors are usually nonlinear with respect to the applied voltage.

$$i_C = C_{OSS}(u)\frac{du_C}{dt} \quad \Leftrightarrow \quad u_C = \frac{1}{C_{OSS}(u)}\int_0^{T_R} i_C\,dt \qquad (1)$$

where

$$C_{OSS}(u) = C_{DS}(u) + C_{GD}(u) \qquad (2)$$

To simplify the error analysis of the sensor influence on the DUT circuit, [1] approximated the mathematical description of a DUT switching current as a linear current ramp tangential to the steepest di/dt of a nonlinear switching current. Similarly, the following calculations approximate the switching voltage (1) as a linear voltage ramp tangential to the steepest du/dt of a nonlinear switching voltage. However, this approach requires two simplifications:

1) The capacitor current is considered as a constant over the duration of the switching event: $i_C(t) := I_C$.
2) The output capacitance $C_{OSS}(u)$ in (1) is replaced by a constant capacitance that stores the same energy as the nonlinear output capacitance $C_{OSS}(u)$ when charged from 0 V to U_{DC}, given by (3).

[1]In most datasheets, the time it takes for the channel voltage to rise from 0 V to the DC value is called T_f, since the definition of "rise" and "fall" correspond to the channel current. To avoid misunderstandings within this article, we'll refer to the rising slope of the channel voltage as Rise Time T_R.

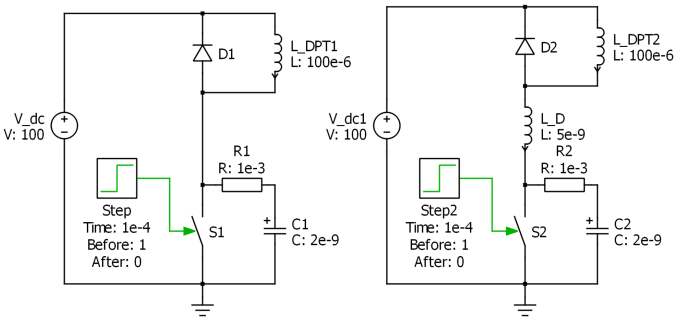


FIGURE 2. PLECS circuit used to validate the simplified switching voltage description (6). Left: Simplified circuit as described in Section II-A. Right: More realistic circuit with parasitic device inductance $L_D = 5$ nH.

A device-specific value for the latter simplification is often provided in power semiconductor datasheets as $C_{O(ER)}$. For this investigation, the use of the constant value $C_{O(ER)}$ is preferable over the nonlinear voltage-dependent real behaviour of $C_{OSS}(u)$, since it is aimed at a worst-case error estimation for a wide range of power semiconductors and voltage probes, not at a precise (and time-consuming) calculation for a given set of devices.

With these assumptions, the switching voltage u_C can be expressed as (6).

$$E_{OSS}(U_{DC}) = \int_0^{U_{DC}} C_{OSS}(u)\cdot u\,du \qquad (3)$$

$$\frac{1}{2}C_{O(ER)}\,U_{DC}^2 \stackrel{!}{=} E_{OSS}(U_{DC}) \qquad (4)$$

$$C_{O(ER)} = \frac{2\,E_{OSS}(U_{DC})}{U_{DC}^2} \qquad (5)$$

$$u_C(t) \approx \frac{I_C}{C_{O(ER)}}t \qquad (6)$$

The validity of these simplifications can be shown through a simple circuit simulation. The left side of Fig. 2 shows

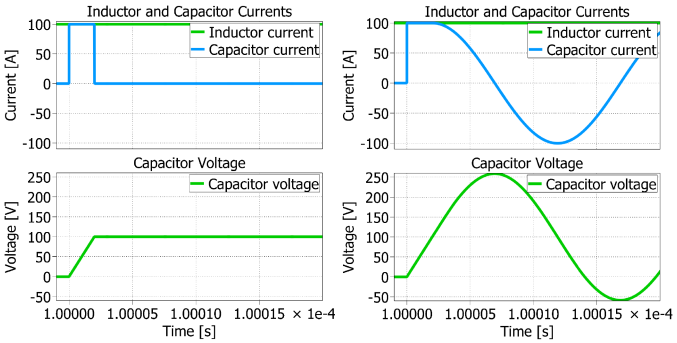


FIGURE 3. Simulation results of the circuits presented in Fig. 2. Left: Simplified circuit as described in Section II-A. Right: More realistic circuit with parasitic device inductance $L_D = 5$ nH.

a simplified circuit as described above while the right side shows a circuit with reasonable parasitic device inductance. The simulation results (Fig. 3) show identical current and voltage waveforms up to the time when the capacitor reaches the DC voltage of 100 V. After this time, the behaviour differs: The simplified circuit shows a constant voltage for its capacitor while the more realistic circuit enters a resonant phase. The frequency and amplitude of this resonance depend on the combination of L_D and C_2, but its du/dt cannot be larger than during the initial capacitor charging process. Therefore, the voltage waveform description (6) is a suitable simplification to describe the capacitor voltage while it is being charged during a turn-off switching event.

To measure this switching voltage in a physical setup, a voltage sensor has to be connected between the channel contacts of the DUT. Most sensors apply a mix of resistive and capacitive voltage dividers to scale the voltage that is applied to its tips down to a level that can be recorded by common data recorders (oscilloscopes) without damage. The geometrical and electrical values of these voltage dividers vary depending on the used sensor. Beside the discrete capacitors that may or may not be implemented in a given sensor, every voltage sensor will at least have some parasitic capacitance between its measurement contacts. For this analysis, the internal structure of these dividers is of secondary importance, as it is sufficient to describe the effective capacitance of the voltage probe that can be measured between its probe tips. The influence of the internal structure of common voltage probes is further investigated in Section IV. Even though the values of the effective capacitance at the probe tips will vary distinctively depending on the manufacturer, type of sensor and its rated voltage, the qualitative effect described below applies to every type of voltage sensor.

The effective capacitance at the probe tips is called C_{Probe}. By connecting a voltage probe to the DUT, this capacitance – be it discrete components or parasitic elements – is connected in parallel to the parasitic capacitance of the DUT. Fig. 4 shows the alteration of the circuit through the insertion of the voltage probe for MOSFET devices and for the simplified switch and capacitance model. The same principle holds true for other types of power semiconductors. Therefore, the

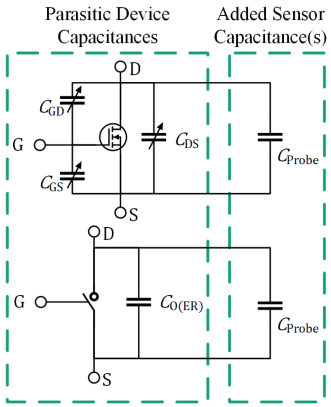


FIGURE 4. Switch capacitance with added sensor capacitance. Top: Real nonlinear device capacitances. Bottom: Simplified energy-equivalent output capacitance.

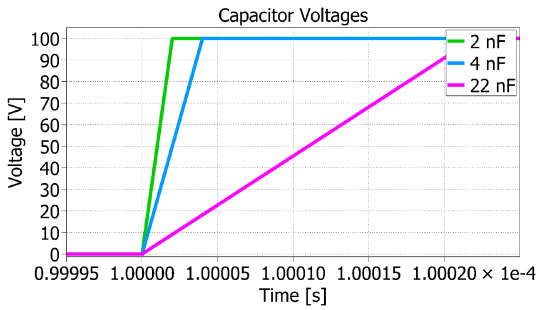


FIGURE 5. Simulation results for the measured capacitor voltge waveforms during a switching event with added probe capacitance of a voltage probe. Green: The same waveform as in Fig. 3 (left). Blue: Simulation result for $C_{\text{Probe}} = C_1$ added to the circuit. Magenta: Simulation result for $C_{\text{Probe}} = 10\,C_1$ added to the circuit.

switching event will not only cause a charging current into the DUT output capacitance $C_{O(ER)}$, but also into C_{Probe} (7). Therefore, the voltage measured between the probe tips will rise slower compared to a circuit without such a probe connected to it, resulting in a larger switching time. This effect can also be validated through simulation as shown in Fig. 5, by modifying the value of C_1 in Fig. 2.

$$u_{\text{DPT}}(t) \approx \frac{I_C}{C_{O(ER)} + C_{\text{Probe}}} t \tag{7}$$

A comparison of the voltage waveform descriptions (6) and (7) with the results presented in [1] concerning the influence of current sensors on switching currents reveals that the alteration of the respective signals is qualitatively identical (see Table 2). We can therefore apply the same error calculation methodology used in [1] to find an equivalent error description for voltage probes, which leads to the Relative Capacitance Alteration Error Γ_C (8).

$$\Gamma_C = \frac{u_C(t) - u_{\text{DPT}}(t)}{u_C(t)} = \frac{1}{\dfrac{C_{O(ER)}}{C_{\text{Probe}}} + 1} \tag{8}$$

This further enables similar conclusions as presented for current sensors, the only difference being a much better

TABLE 2. Comparison Between the Mathematical Descriptions for the Switching Transient Waveforms for Current and Voltage Sensors

	Without Sensor	With Sensor
Current Measurement	$i_0(t) = \frac{U_{DC}}{L_{par}} t$	$i_{DPT}(t) = \frac{U_{DC}}{L_{par} + L_{Sensor}} t$
Voltage Measurement	$u_C(t) = \frac{I_C}{C_{O(ER)}} t$	$u_C(t) = \frac{I_C}{C_{O(ER)} + C_{Probe}} t$
Abstract Function	$f_1(t) = \frac{k_1}{k_2} t$	$f_2(t) = \frac{k_1}{k_2 + k_3} t$

availability of the neccessary data to evaluate this error description for a given DUT/sensor combination: When both the parasitic capacitance of the DUT $C_{O(ER)}$ and the input capacitance of the voltage probe C_{Probe} are identical, the relative error will result to 50 %, in which case the DUT's voltage inside a DPT setup can only rise with a $^{du}/_{dt}$ slope that is half as steep as in the original setup without a voltage sensor. This effect is clearly visible in Fig. 5, comparing the green and blue waveforms. The error will increase for $C_{O(ER)} < C_{Probe}$ and it will decrease for $C_{O(ER)} > C_{Probe}$.

This relationship emphasises the need to make use of voltage sensors with very low input capacitance when trying to measure highly compact and/or fast power semiconductors in a DPT. Considering however that this error is always dependent on the *ratio* of these capacitances, a large error can also be expected for larger DUTs measured with unsuitable voltage probes, i.e. probes posessing a large input capacitance.

B. DISTORTION OF THE SENSOR'S OUTPUT SIGNAL

Most voltage probes used for DPT measurements consist of some sort of RC network to divide the voltage applied to their probe tips. This results in voltage sensors having low pass characteristics. Due to this behaviour, we can calculate the low-pass filter error the same way as presented in [1], by exchanging the original and filtered current functions with the respective voltage functions. The calculation of the filter error is performed by transforming the voltage signal at the probe tips (7) to the laplace domain, multiplying the result with a suitable filter description and by transforming the filtered laplace domain description back to the time domain. This calculation process is visualised in Fig. 6.

Since (7) is only valid over the duration of the measured switching event T_{Probe} and produces a maximum amplitude of U_{DC}, we can further simplify this expression as (9). Note that T_{Probe} is the *measured* voltage rise time, which can be significantly larger than the rise time of a DUT without a voltage probe attached to it (see Fig. 5).

$$u_{DPT}(t) = \frac{U_{DC}}{T_{Probe}} t \tag{9}$$

where

$$\frac{U_{DC}}{T_{Probe}} := \frac{I_C}{C_{O(ER)} + C_{Probe}} \tag{10}$$

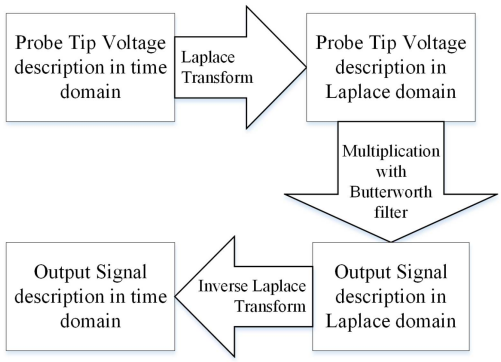


FIGURE 6. Transformation process to calculate the time domain description of the filtered output signal by applying a low-pass filter to the voltage at the probe tips.

Using the transformation approach described above and a first-order butterworth low-pass filter, the sensor output signal calculates to (11), where ω_c is the angular cutoff frequency of the butterworth filter.

$$u_{Filt,1}(t, \omega_c, T_{Probe}) = \frac{U_{DC}}{T_{Probe}} \frac{e^{-\omega_c t} + \omega_c t - 1}{\omega_c} \tag{11}$$

Again referring to [1], the Relative Bandwidth Distortion Error $\Gamma_{Filt,1}$ of the filter effect can be expressed as (12).

$$\begin{aligned} \Gamma_{Filt,1}(\omega_c, T_{Probe}) &= \frac{\int_0^{T_{Probe}} |u_{DPT} - u_{Filt,1}| \, dt}{\int_0^{T_{Probe}} u_{DPT} \, dt} \\ &= \frac{2(e^{-\omega_c T_{Probe}} + \omega_c T_{Probe} - 1)}{\omega_c^2 T_{Probe}^2} \end{aligned} \tag{12}$$

C. TOTAL SENSOR ERROR

The influences described in Sections II-A and II-B form a chain of errors. First, the insertion of the probe input capacitance causes the voltage across the DUT to rise a little slower than in a circuit without such a probe. Then, this slower rising, large signal transient has to be transformed into a small signal output value. Therefore, the chain of errors can also be expressed similar to [1] as a Relative Total Error Γ_{total} (13).

$$\begin{aligned} \Gamma_{total} &= 1 - (1 - \Gamma_C) \cdot (1 - \Gamma_{Filt,1}) \\ &= \Gamma_C + \Gamma_{Filt,1} - \Gamma_C \cdot \Gamma_{Filt,1} \end{aligned} \tag{13}$$

This total error is dependent on the parasitic output capacitance of the DUT $C_{O(ER)}$, the input capacitance of the voltage probe C_{Probe}, its angular cutoff frequency ω_c and on the voltage rise time T_{Probe} of the DUT while a voltage probe is attached to it.

The calculations of both errors can be transferred directly also to turn-on events where the channel voltage decreases from the applied DC value to 0 V, since the only difference would be a DC offset and a negative sign on the voltage slope in (9), which both cancel out in the error calculation (12).

An application of this error calculation to other measurements is possible as well by exchanging the parasitic capacitor

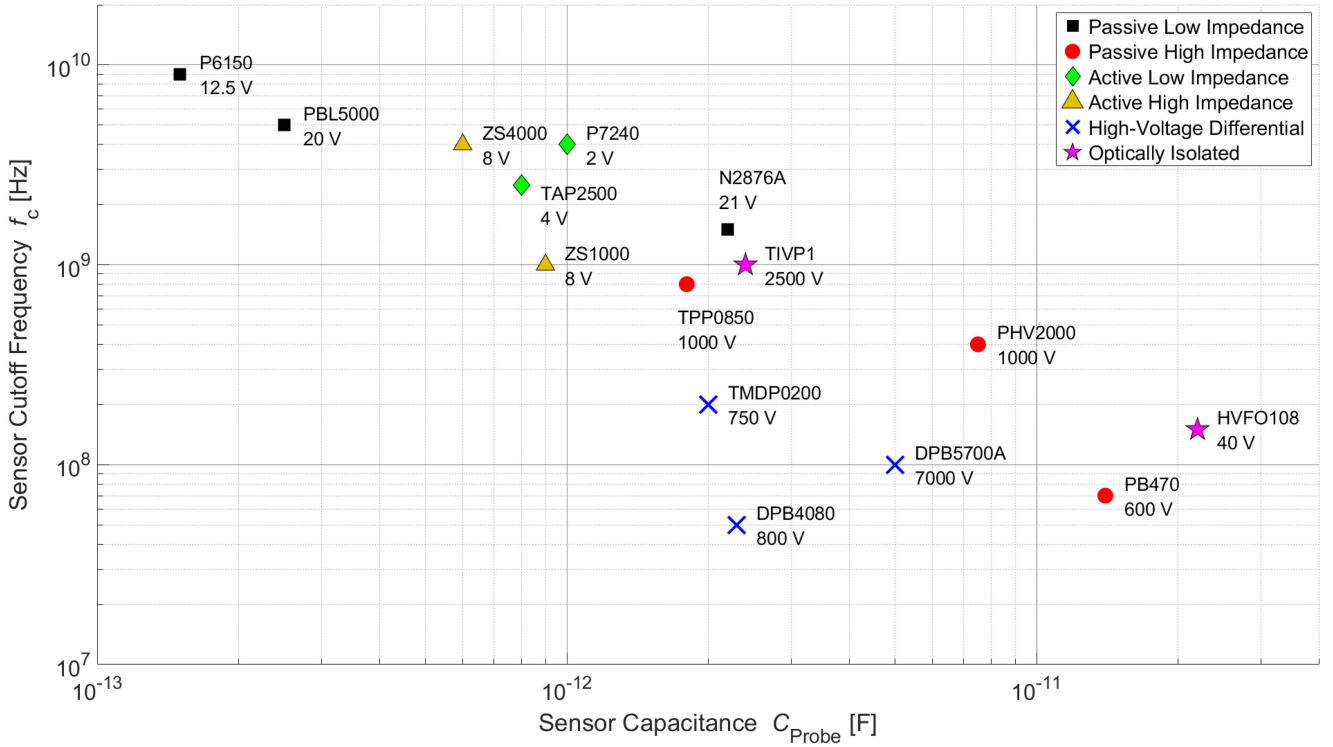


FIGURE 7. Overview of Voltage Sensors with respect to their Bandwidth, Input Capacitance and Maximum Operating Voltage [7], [8], [9], [10], [11], [14], [15], [16], [17], [18], [19], [20], [21].

$C_{O(ER)}$ in (8) with the property of the intended measurement site, e.g. with the parasitic gate capacitance C_{GS} for gate voltage measurements.

III. AVAILABLE SENSOR TYPES

With this error description, it is now possible to compare the performance of available voltage probes for different DPT scenarios. Available voltage probes can be distinguished by their acquisition method – active or passive – and by their input impedance – high or low impedance.

Passive probes commonly use an RC voltage divider network to scale the input voltage down to a level that can be measured with connected data recorders, e.g. oscilloscopes. Active probes make use of operational amplifiers which provide higher input voltage capabilities than passive probes at the cost of usually much lower cutoff frequency.

The input impedance of these probes both influences the cutoff frequency of the probe as well as the maximum allowed input voltage. Low impedance probes enable higher cutoff frequencies than high impedance probes, but can only be used to measure relatively small voltages.

Since passive probes only contain one filter element, i.e. the input RC network, they can be considered as first-order low-pass filters. Active probes on the other hand possess an additional operational amplifier which forms a second filter element, thus resembling second-order low-pass filters.

In reality, the measurement cable which connects the probe output to the data recorder also possesses a cutoff frequency. Since mostly coaxial cables with cutoff frequencies in the GHz range are used for this purpose and since they can be more or less identical for both sensor types, they will not be considered further in this investigation.

Fig. 7 presents a selection of contemporary voltage probes and compares them regarding their sensor input capacitance C_{Probe}, their cutoff frequency f_c and their maximum allowed input voltage. It is clearly visible that across the different sensor types, low-impedance probes enable the highest cutoff frequencies up to approx. 10 GHz and tend to have lower input capacitances, usually below 1 pF, at the cost of a low maximum input voltage. On the other hand, most high-impedance probes provide cutoff frequencies well below 1 GHz and input capacitances decisively larger than 1 pF, while being able to measure several hundreds, if not thousands of volts.

IV. METHODOLOGY APPLICATION AND SENSOR EVALUATION

To provide an impression of practical issues, Fig. 8 presents a selection of discrete SiC and GaN devices as well as SiC modules, comparing them with respect to their output capacitance $C_{O(ER)}$ and their switching rise times T_R. Depending on the combination of power semiconductor and voltage probe, one or both of the presented error mechanisms can play a significant role during data acquisition.

For example, a GaN Cascode TP65H480G4JSG, rated for 650 V/3.6 A [6], which possesses an output capacitance of $C_{O(ER)} = 13$ pF and provides voltage rise times as fast as

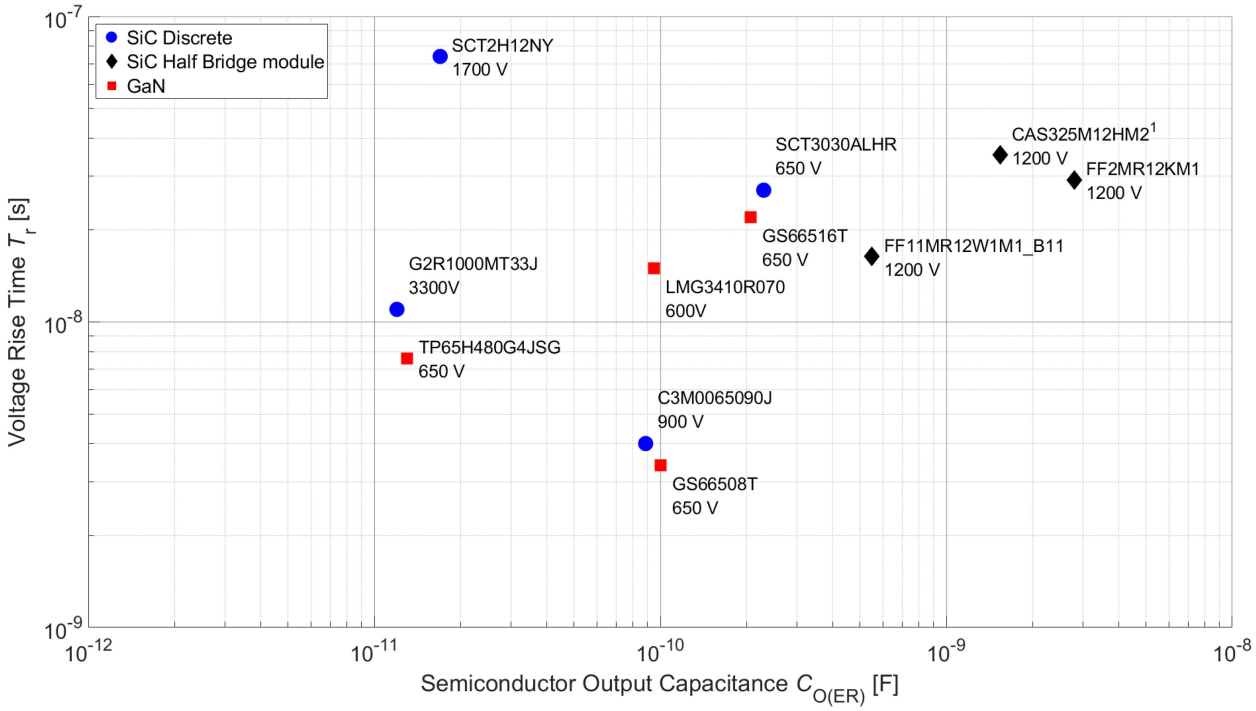


FIGURE 8. **Overview of Power Semiconductor Output Capacitances and Switching Rise Times (Datasheet Values [6], [12], [13], [22], [23], [24], [25], [26], [27], [28], [29]).[1] C_{OSS} used due to missing $C_{O(ER)}$ value.**

$T_R = 7.6\,\text{ns}$, measured with a passive high-impedance probe PHV2000 [7] ($C_{Probe} = 7.5\,\text{pF}$, $f_c = 400\,\text{MHz}$) would result in a Relative Capacitance Alteration Error of $_C \approx 36.6\,\%$ and a Relative Bandwidth Distortion Error of $_{Filt,1} \approx 9.92\,\%$, leading to a Relative Total Error of $_{total} \approx 42.88\,\%$. In other words, such a combination would probably yield unusable results.

Applying the proposed methodology to different voltage probes allows an assessment of whether or not they are suitable for a specific application. Out of the sensors shown in Fig. 7, the following examples are more closely analysed in this article:

- Passive Low Impedance Probe *Yokogawa PBL5000* [8]
  e.g. for gate voltage measurements:
  $U_{max} = 20\,V_{RMS}$ / $40\,V_{AC,Peak}$
  $f_c = 5\,\text{GHz}$
  $C_{Probe} = 0.25\,\text{pF}$
- Passive High Impedance Probe *Tektronix TPP0850* [9]
  e.g. for channel voltage measurements for devices up to 600...650 V breakdown voltage:
  $U_{max} = 1000\,V_{RMS}$ / $2500\,V_{AC,Peak}$
  $f_c = 800\,\text{MHz}$
  $C_{Probe} = 1.8\,\text{pF}$
- High-Voltage Differential Probe *Siglent DPB5700 A* [10]
  e.g. for channel voltage measurements for high-voltage devices up to 6.5 kV breakdown voltage:
  $U_{max} = 7\,kV_{DC + Peak\ AC}$
  $f_c = 100\,\text{MHz}$
  $C_{Probe} = 5\,\text{pF}$
- Optically Isolated Probe *Tektronix TIVP1* [11]
  e.g. for gate and channel voltage measurements:
  $U_{max} \leq 2.5\,\text{kV}$ (depending on probe tip)
  $f_c = 1\,\text{GHz}$
  $C_{Probe} = 2.3 \ldots 28\,\text{pF}$ (depending on probe tip)

Fig. 9 shows the Relative Capacitance Alteration Error $_C$ of each of these probes caused by their added capacitance in parallel to a given power semiconductor output capacitance, while Fig. 10 shows the Relative Bandwidth Distortion Error $_{Filt}$ caused by the limited bandwidth of the sensor.

The total error $_{total}$ can now be calculated using (13). However, a comparison of multiple sensors is difficult to visualise in a single graph, since the total error of every sensor is a curved plane in three-dimensional space. If they were combined, the individual error functions would create cross-sections or overlays, making such a display impractical. One alternative is a representation of a two-dimensional cross-section of these overlays at a given height in the three-dimensional space, i.e. at a given total error. By varying this height, available sensors can be compared across differing precision requirements.

This comparison is performed in Figs. 11 through 13 for the investigated exemplary sensors. Fig. 11 allows relatively high total errors of $_{total} = 10\,\%$, while Figs. 12 and 13 impose lower errors of $_{total} = 5\,\%$ and $_{total} = 1\,\%$, respectively. The curves draw the contour of the three-dimensional error function of each sensor for the given total error. Points to the left and/or below these curves, corresponding to lower device capacitances and/or shorter switching times, result in larger errors for a given sensor than the marked curve. Points above and/or to the right of these curves correspond to longer

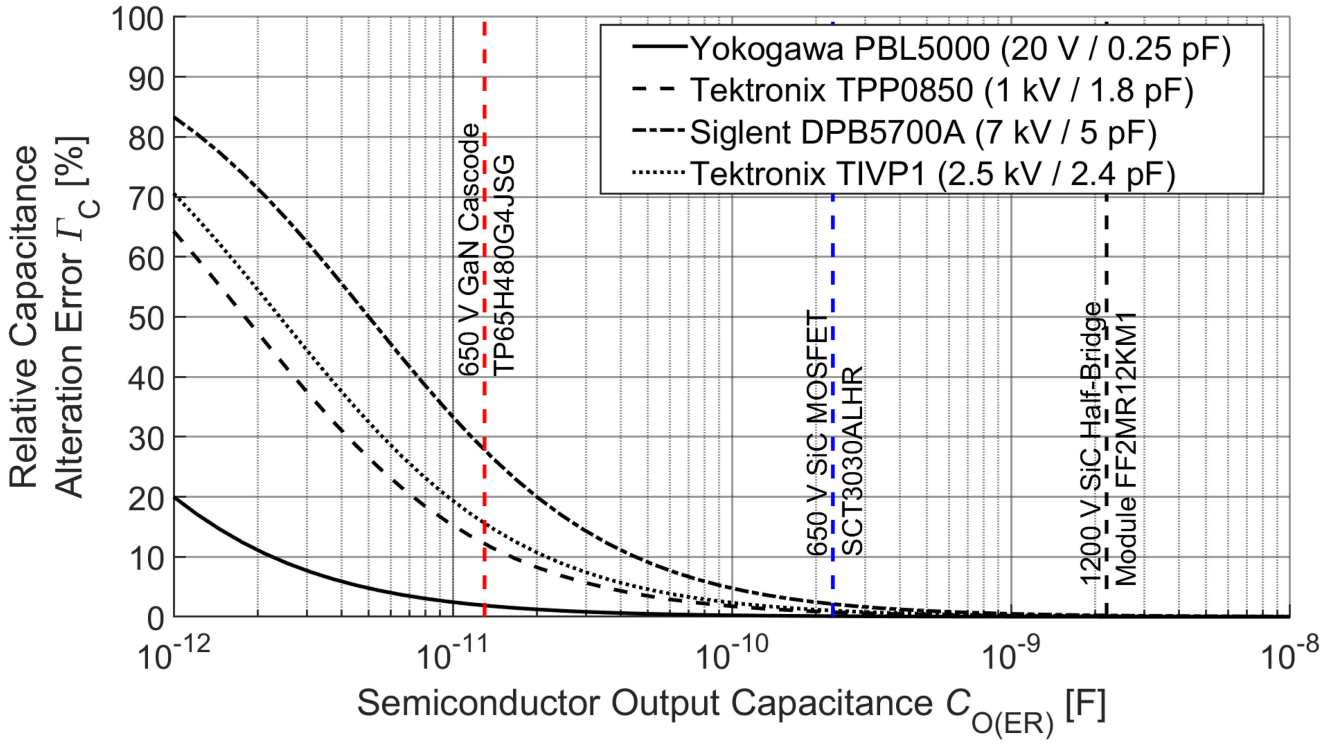


FIGURE 9. Relative Capacitance Alteration Error $_C$ for four exemplary Voltage Sensors [8], [9], [10], [11] and a comparison with three exemplary power semiconductor output capacitances [6], [12], [13].

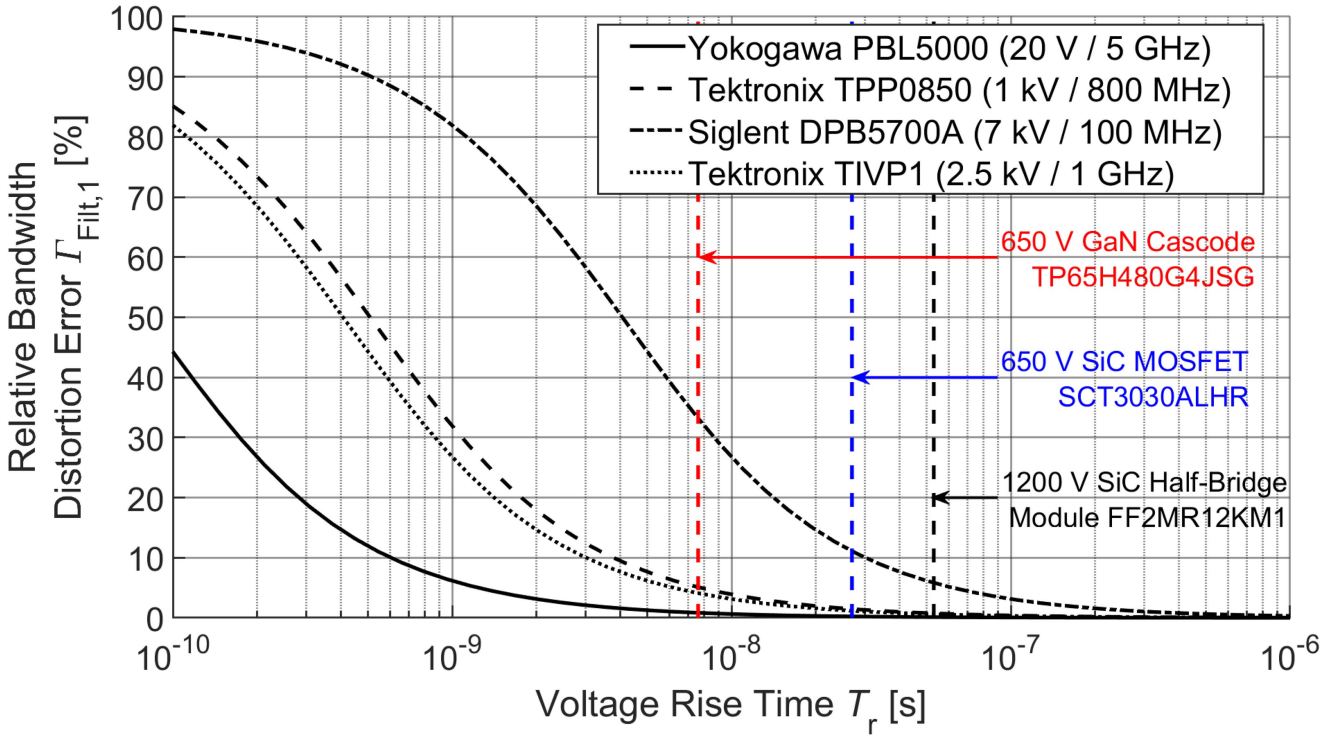


FIGURE 10. Relative Bandwidth Distortion Error $_{Filt,1}$ for four exemplary Voltage Sensors [8], [9], [10], [11] and a comparison with three exemplary power semiconductor switching times [6], [12], [13]. The example switching time values are based on datasheet values. Depending on the application, these devices may switch faster or slower.

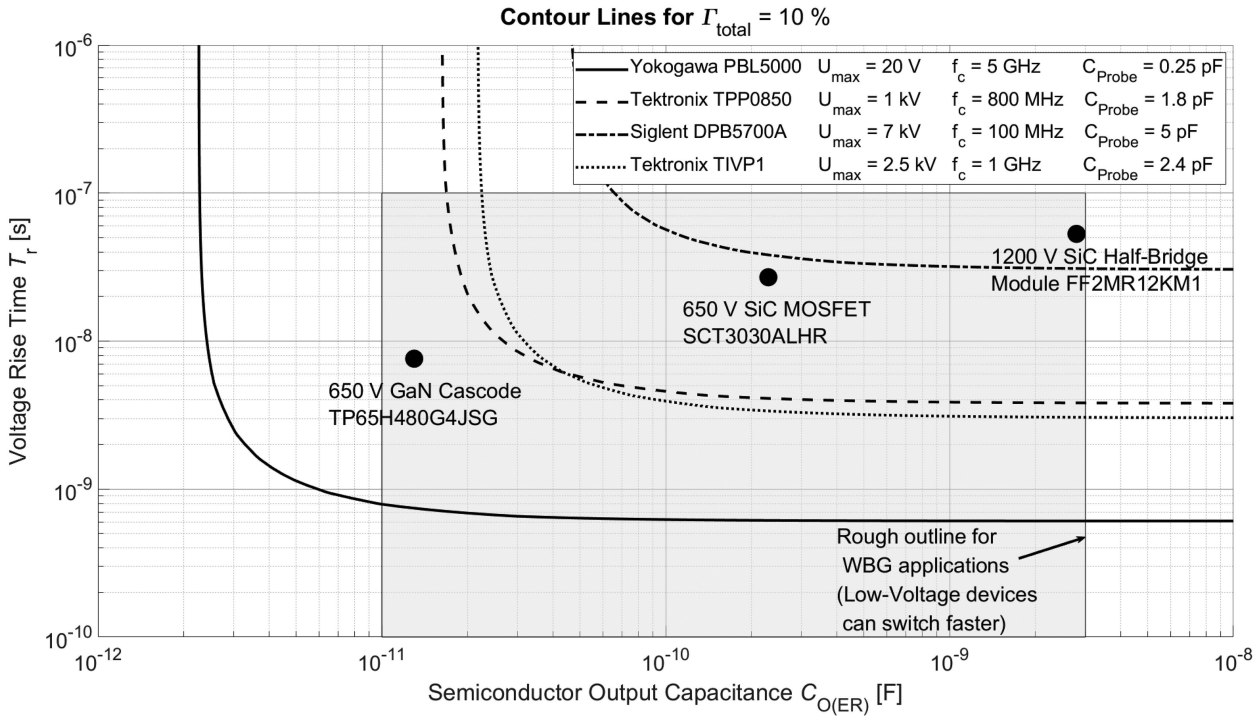


FIGURE 11. Comparison between the investigated Voltage Probes [8], [9], [10], [11] for a maximum total error of $\Gamma_{total} = 10\,\%$. The example values for the three marked power semiconductors are based on datasheet values [6], [12], [13]. Depending on the application, these devices may switch faster or slower, corresponding to lower or higher positions on the vertical axis.

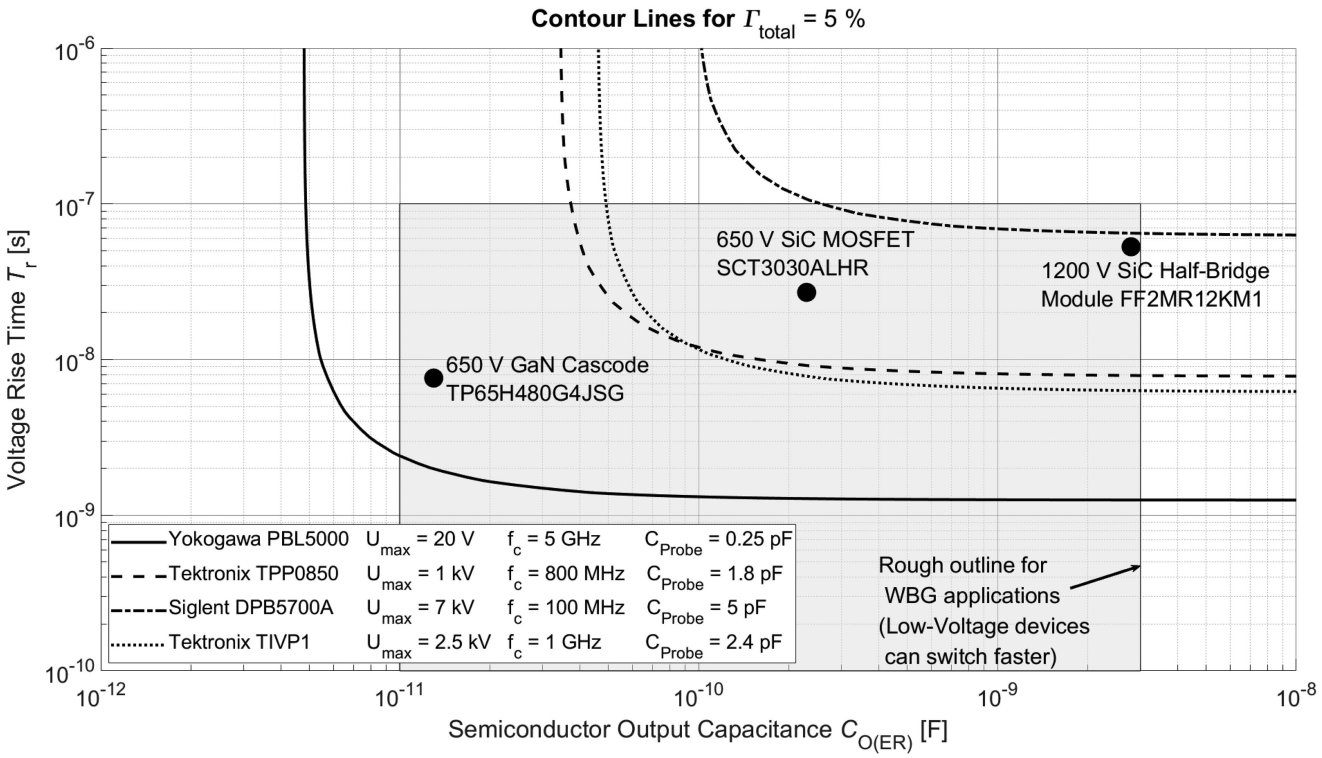


FIGURE 12. Comparison between the investigated Voltage Probes [8], [9], [10], [11] for a maximum total error of $\Gamma_{total} = 5\,\%$. The example values for the three marked power semiconductors are based on datasheet values [6], [12], [13]. Depending on the application, these devices may switch faster or slower, corresponding to lower or higher positions on the vertical axis.

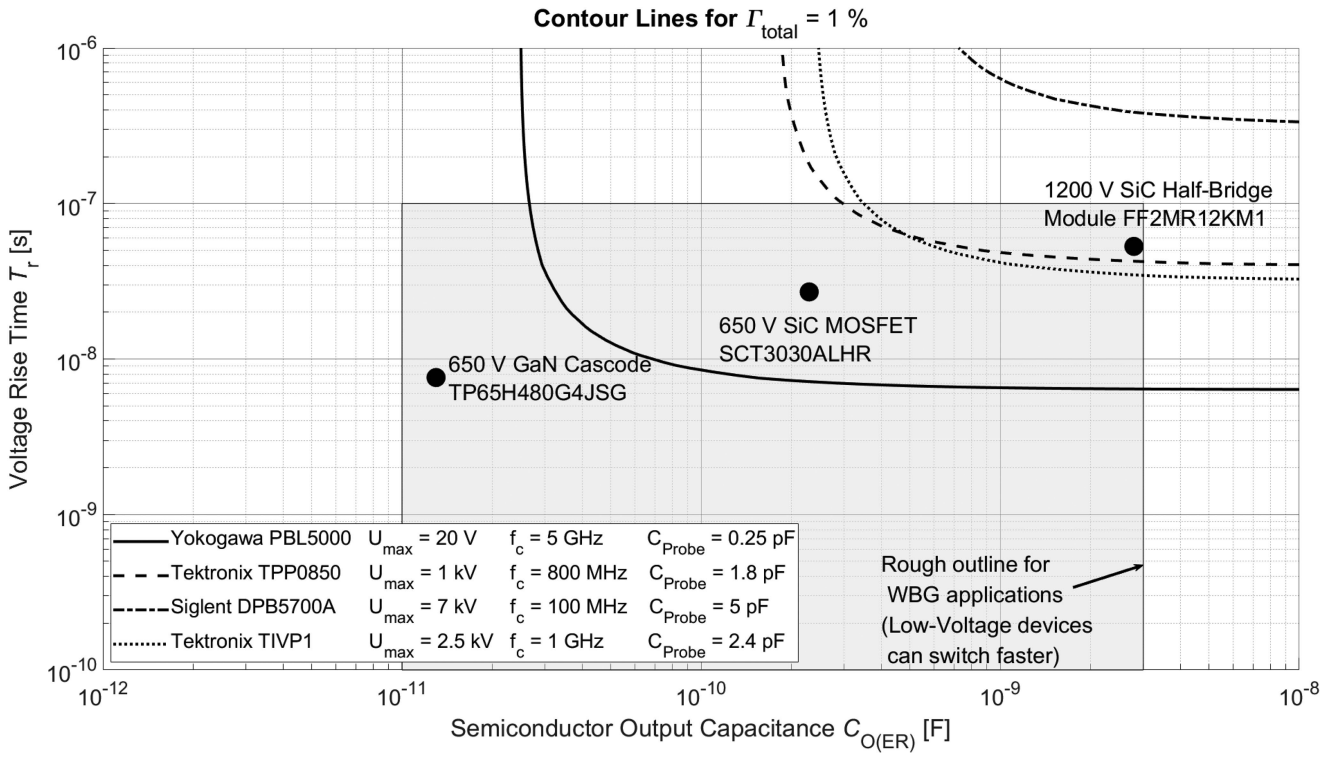


FIGURE 13. Comparison between the investigated Voltage Probes [8], [9], [10], [11] for a maximum total error of $\Gamma_{total} = 1\,\%$. The example values for the three marked power semiconductors are based on datasheet values [6], [12], [13]. Depending on the application, these devices may switch faster or slower, corresponding to lower or higher positions on the vertical axis.

switching times and/or higher device capacitances and result in smaller errors for a given sensor.

The grey box in each of these figures roughly outlines application areas where WBG power semiconductors are usually used, based on the non-complete survey of Fig. 8 and practical experience of the authors. It is to be expected that this area does not cover all available WBG devices and that it will expand to the lower-left side of the graph as device technology progresses.

Since the *Yokogawa PBL5000* (solid line in Figs. 9 to 13) possesses both the lowest input capacitance and the highest cutoff frequency, it can cover the largest application area of all the investigated sensors with relatively low total errors. However, since its maximum input voltage is limited to only 20 V, it can only be used for very low-voltage semiconductors or gate voltage measurements. When fast-switching, low-capacitance semiconductors such as the GaN Cascode TP65H480G4JSG are to be measured, then even this sensor cannot provide total errors below approx. 4 %.

A *Tektronix TPP0850* (dashed line in Figs. 9 to 13) provides decisively lower bandwidth and higher input capacitance, but is able to accept up to 1 kV of input voltage. The *Tektronix TIVP1* (dotted line in Figs. 9 to 13) provides a similar error characteristic, but offers a higher input voltage of up to 2.5 kV and an optical isolation between the probe tip and the oscilloscope. Both of these probes can still cover a wide range of power semiconductors with reasonably low total errors while being able to measure their channel voltages for the 650 V-class. The latter one could also be used for higher-voltage power semiconductors, such as 1200 V or 1700 V devices.

The fourth candidate *Siglent DPB5700 A* (dash-dotted line in Figs. 9 to 13) can handle even higher input voltages of up to 7 kV, but possesses both the largest input capacitance and the lowest cutoff frequency of all investigated voltage probes. It is therefore probably unsuitable for WBG channel voltage measurements, as the resulting total errors would be much larger than with the competitive probes. However, this probe could be well suitable for slower-switching, usually higher-capacitance high-voltage power semiconductors such as 6.5 kV IGBTs that would usually be placed far in the upper-right corners of these graphs.

V. CONCLUSION

While the switching behaviour of most conventional Si power semiconductors can be reliably measured with most sensors, fast WBG devices require the most advanced sensors currently available in order to reduce their impact on the measurement. The combination of low parasitic device capacitance and short switching times is of course beneficial to the system design since it enables a loss reduction and/or higher switching frequencies. However, these properties also pose difficult measurement challenges for a precise device characterisation in a DPT environment, as the parasitic device capacitances approach the

same order of magnitude as common probe input capacitances (see Figs. 7 and 8). At the same time, their switching times become so short that some probes begin to show distortion effects due to insufficient bandwidth.

This paper therefore investigated the effects of voltage probes on the switching behaviour of power semiconductors in a DPT setup and proposed mathematical models to estimate the errors that these influences impose on the DUT circuit when compared to an application where such voltage probes are not connected to the DUT. These error calculations were then applied to available exemplary voltage probes and the results were discussed.

The developed error models provide a method that enables a quick estimate of the suitability of voltage sensors for a given measurement task, requiring only the cutoff frequency and input capacitance of the voltage probe as well as the switching time and parasitic device capacitance of the power semiconductor that is to be measured.

One drawback of the developed method is the fact that the switching time of the DUT has to be known in advance, which requires a measurement of said switching time in the first place. Since this measurement would be subject to the same error mechanisms described in Section II of this work, these values have to be treated with care, as switching times in an application without voltage probes will be faster than the measured values. However, there is no measurement technique that can correctly "guess" the real switching time of a power semiconductor without influencing its switching behaviour.

The worst case approach of the proposed error estimate, approximating the switching transient through a straight line tangential to the steepest $^{du}/_{dt}$, will probably be close enough or even shorter than the switching times in practical applications, so that this approach provides the best approximation available.

With the error calculations for current sensors presented in [1] and the corresponding investigations for voltage probes presented in this article, there are now worst-case analyses available that evaluate and rate the influence of such probes on the switching behaviour of power semiconductors. These analyses could be improved in the future by selecting more realistic mathematical waveform descriptions for the respective transients so that the difference between the selected description and real switching events decreases. However, this approach will likely cause more complex mathematical error descriptions and will require different descriptions for the available types of power semiconductors (IGBTs, MOSFETs, BJTs etc.). Additionally, since these investigations focus on each of the necessary sensors individually, future research should analyse their combined influence in a DPT environment more closely, both with respect to their cross-influence on each other as well as concerning the consecutive calculation of switching losses that is based on their output signal.

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