Addressing Low-Power Electronics in a Digital System and FPGA Design Course

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***Abstract*— Low power dissipation is a current topic in digital design, and therefore, it should be covered in a state-of-the-art electrical engineering curriculum. This paper describes how low-power design can be addressed within a digital design course. Doing so would be beneficial for both topics because low-power design is not detached from the systems perspective, and the digital design course would be enriched by references to current challenges and applications. Thus, the presented course should serve as an example of how a course can be developed to also teach students about sustainable engineering.**

***Index Terms*—low power; education; energy awareness; FPGA**

I. INTRODUCTION

Lecturers constantly have to review whether the courses they teach cover the relevant content in a changing world. At our university, the study programs of mechanical and electrical engineering are currently revised to consider sustainable development. This initiative is called the "Blue Track", where blue stands for efficiency and responsible use of resources [1].

In the area of digital design an important aspect of sustainability is to the power dissipation of integrated circuits. Students are aware of the need for sustainability and energy conservation, and accordingly, they will expect the issue of power dissipation to be addressed in their courses [2-4]. But sustainability is not an end in itself. Low power dissipation allows long running times for battery-powered devices and can reduce the need for cooling in electronic systems.

This paper describes an approach by which low-power electronics can be addressed within a digital design course instead of being offered as a supplementary subject, as criticized by [5], or as a special focus course [6]. An advantage of integrating this topic into the course is that it should foster greater interest amongst the students for both aspects, in that energy efficiency will not be presented as a separate subject and digital design will be supplemented with state-of-the-art references and applications.

II. EDUCATIONAL SETTING AND OBJECTIVES

A. Review of digital design textbooks

Digital design is a common topic in an electrical engineering curriculum. A number of English and German language textbooks [6-15] were reviewed in order to determine the content that is proposed for this subject. Five subject areas were identified. Most textbooks do not cover all subject areas, but focus on some of them.

1) Fundamentals

Boolean logic, switching algebra, number systems, digital building blocks (gates, flip-flops), combinational and sequential circuits.

2) Hardware description language

VHDL or Verilog.

3) Digital systems

Hardware implementation, including ASICs (application-specific integrated circuits) and FPGAs (field-programmable gate arrays), memory, embedded system.

4) Microelectronics

MOS transistor theory, manufacturing, cell layout.

5) Low power design

Sources of power dissipation, optimization of power consumption at transistor, logic and system level.

It can be observed that subject area 5, low power design is covered as a special topic [6,11], in combination with area 4, microelectronics [15], with area 3, digital systems [10], or both areas [9].

B. Eductional Setting

In the electrical engineering bachelor's curriculum of the Bonn-Rhine-Sieg University the following digital design modules are offered:

- 3rd semester: Fundamentals of digital design (compulsory)
- 4th semester: Digital design project using FPGAs (elective)
- 6th semester: Power-efficient digital systems (elective)

The 5th semester is reserved for work placement and study abroad, and therefore, there are no lectures.

The compulsory 3rd semester module covers fundamentals of digital design (subject area 1) and an introduction to VHDL (area 2, partially) and FPGAs (area 3, partially). Lectures are supported by a hands-on lab with VHDL and FPGAs. This module is similar to the courses offered at other universities. The hands-on experience can be continued and deepened through a more complex elective FPGA project offered in the 4th semester (area 2 and 3).

C. Educational Objectives

To select the topics for the 6th semester module "Power-efficient digital systems," it is necessary to take into account the career options and requirements of the future scope of work for students of electrical engineering (see also [16]).

Digital designers often develop electronic systems using application-specific integrated circuits (ASICs) and commercially available off-the-shelf components. Because of the considerable effort required for ASIC design, it is preferable to use available components including microcontrollers and FPGAs.

During product specification, design engineers frequently need to estimate the "cost" of a specification; this includes not only the financial budget and the required project time but also the power dissipation. Most digital designers can select among various semiconductor technologies or devices designed using these technologies.

During product design, a digital designer implements the different function blocks of a system. When choosing how to implement a block, the performance, including power dissipation, for alternative implementations must be considered.

In contrast, only few graduates of a bachelor's degree course are expected to work on developing actual semiconductor technologies (area 4). This knowledge is too specialized to justify detailed focus on it in the bachelor's degree program. Instead, this area could be taught by a specialized master.

Thus, the 6th semester course picks up the fundamentals from the 3rd semester and widens this knowledge from the viewpoint of digital systems (subject area 3), including consideration of power consumption (area 5).

III. POWER DISSIPATION OF CMOS CIRCUITS

A. Physical Causes of Power Consumption

Most digital circuits are implemented using CMOS (complementary metal-oxide semiconductor) technology. In these, there are three causes of power consumption, which are leakage currents, charging and discharging of load capacitances resulting from switching of circuit nodes, and short circuit currents during signal transition. The largest contribution normally comes from charging and discharging of load capacitances but with modern CMOS technology and shrinking feature sizes leaking currents increase significantly [6].

The dynamic power consumption depends on the supply voltage, the frequency of the circuit, the load capacitance and the switching factor of the individual circuit nodes [6]. The load capacitance of a node is the capacitance of the interconnections and input transistors addressed by the node. The switching factor is the probability per cycle that a node will switch its value. Some nodes will have a high switching factor (e.g., a program counter in a CPU where the lowest bit changes almost every cycle), whereas other nodes will change relatively infrequently (e.g., the interrupt signal).

B. Influencing Factors to Power Consumption

Low-power design is an active area of research in which several approaches for reducing the power consumption of a digital system are proposed [6]. The following factors determine the power consumption of a digital system.

1) CMOS Technology

The CMOS technology determines the leakage currents, supply voltage and the load capacitances. Reducing the supply voltage is an attractive measure, as it has a quadratic effect in the power dissipation. Lower capacitances can be achieved by reducing feature sizes, e.g., by using a 22 nm CMOS process instead of a 45 nm process. The geometry of transistors for a given technology can be modified in order to trade speed for power as well as to reduce leakage current.

2) System Specification and Architecture

The power consumption of a circuit also depends on its complexity. The more functionality and computing power a circuit has, the larger it will be, and the faster it will need to operate. If the choice of circuit architecture can reduce or eliminate access to external memories, driving of high-capacitance inter-chip connections can be avoided.

3) Circuit Design

Design decisions determine the complexity of a circuit and can influence power dissipation in a manner similar to specification decisions. Using fewer circuit nodes or nodes with only short local interconnections can reduce the load capacity that needs to be switched. Further power reduction can be achieved by lowering the switching activity at the circuit nodes [17]. Current microprocessors do this by switching off unused sections in standby mode.

IV. COURSE DESCRIPTION

The module "Power-efficient digital systems" will combine advanced digital design and low-power electronics. It will be structured into several topics, for each of which a combination of a general digital systems viewpoint and a focus on power dissipation is intended. The topics pertaining to low-power electronics are selected based on the described influencing factors for power consumption as well as on [5] and textbooks covering this subject area [6,9,10,11,15].

The course comprises 10 lectures of 3 hours each. The topics covered in the lecture and their specific low-power focuses are listed below, with the general digital systems topics indicated by "Sys" and the low-power focus indicated by "L-P".

- Introduction
  - Sys: Introduction to CMOS technology
  - L-P: Motivation for low power, source of power dissipation, thermal design power
- CMOS technology
  - Sys: CMOS layout, technology scaling
  - L-P: Transistor design, choice of supply voltages
- Circuit structure
  - Sys: Timing, pipelining, parallel processing
  - L-P: Role of structure for power dissipation, switching activity, clock gating, path balancing
- System architecture
  - Sys: Memory and memory hierarchy, multi-chip modules
  - L-P: Role of architecture for power dissipation
- Embedded system
  - Sys: Introduction to embedded systems, embedded CPUs, use of intellectual property (IP)
  - L-P: Role of embedded software for low power
- Design flow
  - Sys: ASIC/FPGA design flow, verification
  - L-P: Low-power electronic design automation
- System implementation

- Sys: ASIC/FPGA comparison
- L-P: Sleep modes, dynamic adaptation of power dissipation

For some of these lectures, the topics pertaining to general digital systems and the low-power focus are closely related. This is the case for "CMOS technology," where the general introduction of the technology is continued and deepened with the role of technology parameters for power dissipation and performance. Similarly, for "Circuit structure," pipelining is related to switching activity and path balancing.

However, for other lectures, the two sets of topics are more loosely related. For example, "Design flow" has a clear focus on the system part, especially with regard to verification. Low-power design automation is not of equal importance, but it is addressed to a smaller extent to complement the system part.

V. SUITABILITY OF FPGAS FOR HANDS-ON LAB

A. Hands-on Lab with FPGAs

To supplement lectures, students should also be able to work with digital systems [18] and get hands-on experience with power dissipation. FPGAs have been used in the 3rd semester module and are known by students. Therefore, it is desirable to use them also as a platform for lab exercises in the 6th semester module. Ten hours of lab exercises in two or three sessions are provided.

To derive the concept for the hands-on lab, it is investigated whether FPGAs can be used to experience different power consumption. In [19] it is shown, that the FPGA implementations of different security algorithms give measurable differences in power dissipation. The estimation tool of the FPGA supplier gives a pessimistic estimate compared to measurements [19] so it is no substitute for a lab exercise.

In this chapter it shall be investigated how different implementations can be used in a lab exercise so that students can make experiments on power consumption. Different versions of a test circuit are implemented on an FPGA and the power consumption is compared.

B. Experimental Setup

An evaluation board using a Xilinx Spartan-3 FPGA (XC3S400) manufactured in a 90 nm CMOS technology is used in the experimental setup. On the FPGA several instances of a digital circuit (Figure 1) are implemented. A slice of the test circuit consists of an 8bit counter from 0 to 254 and an xor-function to combine the counter value with the result of the previous slice. Counting to 254 instead of 255 was made on purpose to include logic for restarting the counter. Flip-flops store the counter value and the xor result.

The test circuit is designed to provide a certain activity on the FPGA so that the resulting power consumption can be measured. The design is relatively easy to understand and to be modified by students. The flip-flops can be enabled to switch activity on or off.

The circuit does not claim to be a representative implementation of a typical FPGA design, and does not contain memory blocks or multiply units. Nevertheless it uses the main components of an FPGA, i.e. look-up tables (LUT) for arithmetic and logic as well as flip-flops (FF).

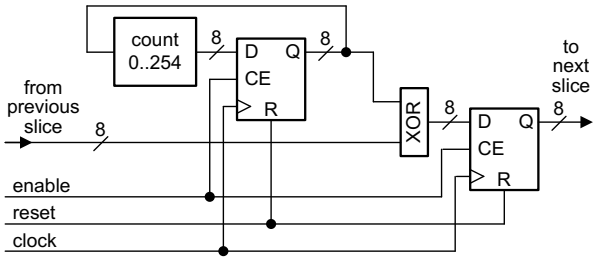

Figure 1. Slice of test circuit for power measurement

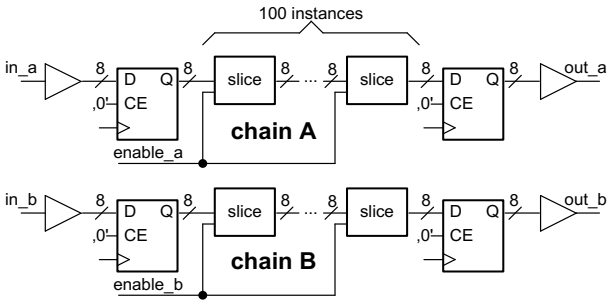

Figure 2. Complete test circuit for power measurement

C. Design Experiments

Four different designs were implemented with the test circuit. They use the same VHDL source code but different design constraints. 200 slices of the test circuit are implemented in two parallel chains, called A and B. Both chains of 100 slices can be enable or disabled. Input and output of the chains are assigned to specific locations but signals on these i/o-flip-flops are disabled by a control switch (Figure 2).

The complete design uses 53% of the LUTs, 45% of the FFs and 73% of the slices. So the FPGA is well utilized but not completely packed, leaving the EDA tool (Electronic Design Automation) freedom for placement and routing. Xilinx ISE 14.6 is used as the EDA tool.

1) Design 1

The evaluation board provides a 66 MHz clock, therefore, the design is implemented with a 15 ns timing constraint. The input pins to both chains are positioned to the left side of the FPGA and the output pins to the right side. Input to chain A is above chain B while the output of chain A is below chain B. Therefore it is expected that the routing of the chains cross each other on the FPGA.

A look at the placement confirms this expectation. Figure 3 shows the routing of chain A and B as two screenshots from the EDA tool. The placement corresponds to a typical FPGA routing, where subcircuits are not constrained to specific regions.

2) Design 2

Design 2 has been implemented with tighter timing constraints, in order to force the EDA-tool to implement a slightly different routing. As design 1 achieves a worst case timing of 12.7 ns the constraint for design 2 was set to 10 ns. This timing is reached without difficulties, giving a worst case timing of 9.9 ns. The routing is nearly identical to design 1 (and thus not presented as a Figure).

3) Design 3

A further option with significantly different routing was implemented. In design 3, the FPGA is divided in regions,

arranged as horizontal bands. All slices of chain A are constrained to the middle band, so the routing should be uncomplicated. However, for chain B all even slices are constrained to the top band and all odd slices are constrained to the bottom band.

Consequently, for chain B, the routing between the slices results in comparatively long connections. Figure 4 shows the routing for both chains. The long connections for chain B can easily be identified, crossing the middle band. The timing constraint of 15 ns (like design 1) is reached without problems, giving a worst case timing of 12.2 ns.

4) Design 4

In this option only chain A is implemented on the FPGA. Chain B is omitted, so the design uses 26% of the LUTs, 22% of the FFs and 36% of the slices. The resulting placement (Figure 5) follows a meandering route in a similar manner as for design 1.

D. Power Consumption of Design Experiments

For all design options, the power consumption of the FPGA is analyzed by measuring the current for the 1.2 V core power supply. The voltage is not measured, but assumed to be stable. This assumption was made with a lab exercise in mind, where only the supply current shall be measured. The experimental setup is depicted in Figure 6 showing the FPGA board (Avnet Xilinx Spartan™-3 400 Evaluation Kit) and the ampere meter.

When both chains are disabled a core current of $I_{core,0}$ = 39.0 mA is measured, which corresponds to a power consumption in the core of $P_{core,0}$ = 46.8 mW. This base consumption results mainly from leakage currents [20] and the clock network of the FPGA, which is not disabled.

Then the power consumption of chain A enabled, chain B enabled and both chains enabled is measured for a clock frequency of 66 MHz. The base consumption is subtracted to get the contribution from the test circuit. For design 1 the following current and power consumption was measured.

- Chain A: $I_{core,A}$ = 23.5 mA ⇒ $P_{core,A}$ = 28.2 mW
- Chain B: $I_{core,B}$ = 23.5 mA ⇒ $P_{core,B}$ = 28.2 mW
- Chain A, B: $I_{core,AB}$ = 45.5 mA ⇒ $P_{core,AB}$ = 54.6 mW

The measurements show that chain A and B give the same increase in power consumption of 28.2 mW and both chains combined give about the sum of the individual increases. The combination of chain A and B ($P_{core,AB}$ = 54.6 mW) consumes slightly less power than the expected sum ($P_{core,A} + P_{core,B}$ = 56.4 mW), probably due to a slight voltage drop.

Design 2 (10 ns timing constraint) runs also with 66MHz and gives current readings which are the same as for design 1 within a margin of 0.1 mA. So the slightly tighter constraint does not led to higher or lower power consumption.

Design 3 (area regions) however results in significantly higher power consumption. The consumption of chain A (center rows) was 12% higher than in design 1, the consumption of chain B (top/bottom rows) 85% higher. This is a consequence of the long connections between top and bottom of the FPGA.

The increase for chain A is attributed to the fact that the long interconnections block routing channels, so that also

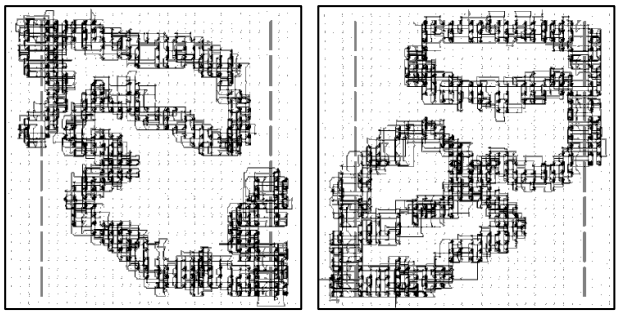

Figure 3. Interconnections of chain A (left) and B (right) in design 1

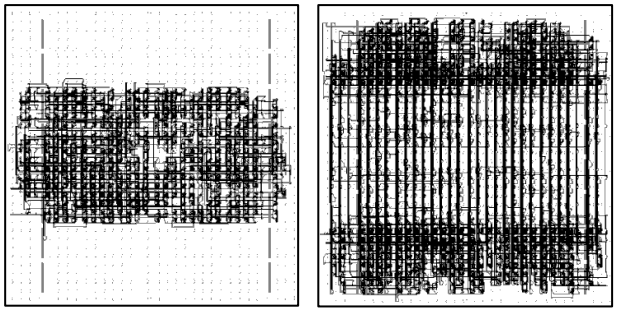

Figure 4. Interconnections of chain A (left) and B (right) in design 3

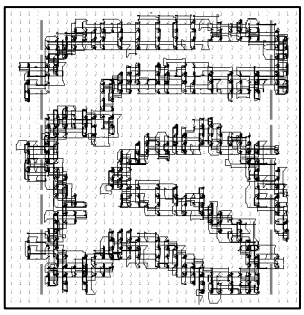

Figure 5. Interconnections of chain A in design 4

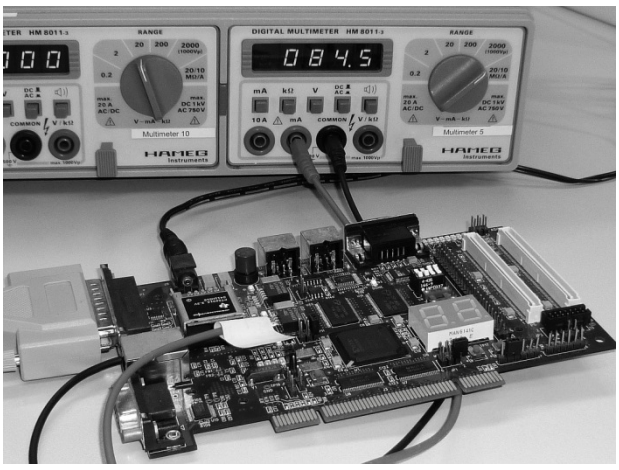

Figure 6. Experimental setup with FPGA board and ampere meter

for chain A slightly longer routing paths are chosen by the EDA tool. Referring to the total power consumption $I_{core,0} + I_{core,A}$, i.e. including the base consumption, the increase is 4%. This is well within the margin observed by [19] where different implementations of a design led to a difference of up to 10% in power consumption.

Design 4 (only chain A) has a lower core current of $I_{core,0}$ = 33.2 mA when the chain is disabled. This can be

attributed to less leakage for a smaller FPGA-usage and less consumption on the clock network which drives fewer FFs. The current and power consumption of chain A is nearly identical to design 1: $I_{core,A}$ = 23.4 mA ⇒ $P_{core,A}$ = 28.1 mW

From this measurement results it can be concluded, that an FPGA is well suited to compare the power consumption of different design implementations in a lab exercise. Slightly different routing of a design gives nearly the same power consumption and a design that is twice as large, gives about twice the power consumption. Also, if long interconnections are present in a design a substantial change of power consumption can be observed by students.

As a reference, Table I gives the complete measurement results. All values are total core currents, i.e. result from base consumption plus contribution from the chains of test slices.

E. Observability of Further Parameters

As a further experiment it was investigated whether a change of power consumption due to different FPGA temperatures can be observed. In an industrial application probably a climate chamber would be used. For a lab exercise a much easier setup is envisaged. The FPGA is cooled down with ice spray, as it is used for debugging of electronic circuits.

Using design 1 with both chains enabled, the FPGA was cooled for seven seconds with ice spray. The core current dropped from 84.5 mA ($I_{core,0} + I_{core,AB}$) to 78.1 mA which is an 8% decrease. Thus, a temperature effect on power consumption is observable for students and can be implemented as an experiment on circuit technology.

VI. DEVELOPMENT BOARD FOR LAB EXERCISES

In the lab exercises students will perform circuit implementations on a programmable circuit and measure the power dissipation of different implementation alternatives. In order to undertake instructive laboratory exercises, students must be able to perform various implementations of a task and measure the resulting power dissipations.

In addition to the test circuit of the previous chapter, students shall work on a practical problem, as this is a more motivating exercise. A certain switching activity inside the FPGA is required in order to measure differences in power dissipation between different implementations. This activity shall be provided by an input signal that can be processed by the FPGA.

For the hands-on lab, video signals have been chosen as input signals. These signals have high frequencies in the range of 100 MHz. Image processing blocks (e.g., filters) are available as intellectual property (IP). Furthermore working with video signals is motivational for students as images are relatively easy to observe using an LCD monitor. Lab exercises can involve the use of filters of different complexity, where the more complex filter will result in better image quality but higher power dissipation. These circuits will also use memory blocks and arithmetic modules of the FPGA which were not used in the simple test circuit. Another exercise can involve the implementation of energy-aware arithmetic units [5].

A development board for the lab session has been developed (Figure 7) [21]. It has video input and output interfaces and the video signal is processed by an FPGA.

TABLE I.
MEASURED CORE CURRENTS FOR TEST CIRCUIT

design	total current in mA			
	chains disabled	chain A	chain B	chain A + B
	$I_{core,0}$	$I_{core,0} + I_{core,A}$	$I_{core,0} + I_{core,B}$	$I_{core,0} + I_{core,AB}$
design 1	39.0	62.5	62.5	84.5
design 2	39.0	62.6	62.6	84.6
design 3	38.9	65.2	82.4	105.8
design 4	33.2	56.6	-	-

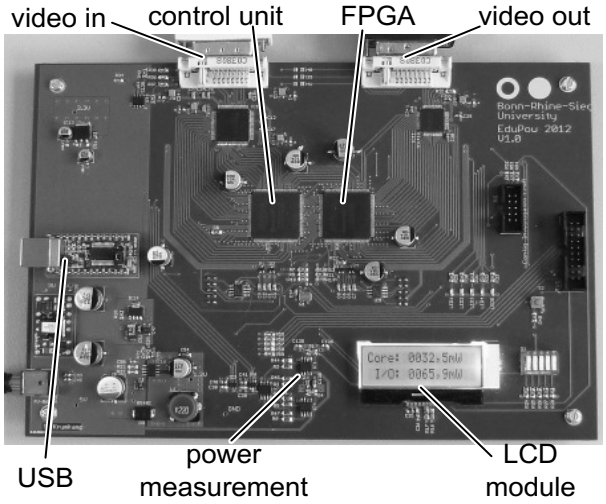

Figure 7. Development board for low-power education

The power consumption of this FPGA is measured and will be compared by students. A control unit, which is also an FPGA, is used for selecting the input signal and calculating the power consumption the system. The result of the power measurement can be displayed on an LCD module or transmitted by USB.

A prototype of the development board is available and will be used to gain teaching experience. Based on the feedback of students, the specification of the board will be improved.

VII. CONCLUSION

Advanced digital design and low-power electronics are combined in a new 6th semester course "Power-efficient digital systems" that is currently being developed. Fundamental knowledge about semiconductor technology and digital systems shall be combined with relevant aspects of low-power design in a way that is beneficial for both topics. This course serves as an example of how a lecture can be developed to include teaching about sustainable engineering.

It has been shown that lab exercises using an FPGA allow measuring the power consumption resulting from design decisions, like circuit complexity or routing. Also experiments on circuit technology are possible, like temperature effects on semiconductor behaviour. Different implementations of image processing algorithms, like filters, can show the trade-off between image quality, circuit complexity and power consumption. An FPGA-based development board has been implemented and will be used in lab exercises and for student projects.

Nevertheless, it must be noted that the FPGA is merely a platform for circuit implementation and the lab exercises teach students about general low-power circuit structures.

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